

CADENCE TRAINING

IIT Gandhinagar

Date: 29th November – 3rd December, 2010

Timings: 9:30 am to 5:30pm

Venue: Computer lab, L-Block, IIT Gandhinagar

Conducted by: Mr. R. Bhanuprakash and Mr. Santosh V. R. Avancha

Course Schedule

30th November 2010

Virtuoso DFII environment, Virtuoso Schematic Editor, Schematic level implementation of Differential Amplifier, Advanced analysis using Virtuoso Spectre Circuit simulator, Virtuoso Analog Design Environment (ADE) AMS simulation, Statistical analysis (Monte-Carlo simulations of designs), Power estimation (static, dynamic, leakage), Corner analysis (4-corner simulation).

1st December 2010

Virtuoso Layout Editor (schematic to layout and routing using tool), Assura Physical Verification, Assura parasitic Extraction, Post-layout simulation using all views (av_extracted etc), CDB to OA conversion Noise analysis.

2nd December 2010

Incisive Unified Simulation - For RTL Code (Verilog Codes) functional Simulation and explore various features of the tool. Encounter RTL Compiler. Gate level synthesis of two RTL designs: 1. Serial adder circuit and 2.DTMF chip design.

3rd December 2010

Encounter digital implementation. (For ASIC Physical Design): Floorplan to Parasitic Extraction and signoff timing simulation of DTMF chip design. Post-layout Simulation using ETS: Dedicated Timing simulation and cover basics of SI and Power Analysis using ETS.